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Result # 1 Relevance:

A method to improve interrupt response latency for multi-processor systems is disclosed. The method includes: receiving an interrupt signal; determining a processor to handle the interrupt; and dispatching the interrupt to the processor. The method is implemented in a multi-processor system. **English**
2004-02-09 IPCOM000021781D

Disclosed is a method to improve interrupt response latency in a multi-processor system. The method includes: receiving an interrupt signal; determining a processor to handle the interrupt; and dispatching the interrupt to the processor. The method is implemented in a multi-processor system. **English**

Result # 2 Relevance:

Balanced Handling of I/O Interrupts in a Multiprocessor System
1993-02-01 IPCOM000103860D **English**

A method for handling I/O interrupts in a multiprocessor system is disclosed. An algorithm is disclosed which: (1) allows any processor in the system to handle an I/O interrupt, (2) prevents a processor from waiting on a processor that will not be in a position to handle it ...

Result # 3 Relevance:

Programmable Interrupt Vectors in Processors
1982-10-01 IPCOM000050438D **English**

Described is a method to select under program control the vector number of an interrupt. The method includes: receiving an interrupt signal; determining a processor to handle the interrupt; and dispatching the interrupt to the processor. The method is implemented in a multi-processor system. **English**

Result # 4 Relevance:

Interrupt Protocol for Interconnected Microprocessors
1978-07-01 IPCOM000070026D **English**

Microprocessor 10 drives address bus 11 and data bus 12, which are also coupled to memory 13. Microprocessor 14 and to a set of addressable registers 20. Another microprocessor 30 drives address bus 31 and data bus 32, which are connected to another memory 33, to other ...

Result # 5 Relevance:

Method for dedicated CPU interrupt tasking
2004-04-22 IPCOM000028085D **English**

A method for dedicating one or more processors in a multiprocessor system or logical processor to dedicated device interrupt handling, thereby reserving a known quantity of processing capacity for dedicated workloads.

Result # 6 Relevance:

Technique to Passively Interrupt a Processor
1991-03-01 IPCOM000119856D **English**

Operating systems have the need to maintain status regarding facilities that are external to the processor (e.g., I/O devices). There are two basic approaches, namely, having the device generate an interrupt instruction execution or having the operating system actively poll the device for status. **English**

Result # 7 Relevance:

Apparatus to Download and Verify Microcode onto Multiple Processors
1993-12-01 IPCOM000106619D **English**

Disclosed is an apparatus to download multiple pieces of microcode onto a system that includes multiple processors and multiple pieces of memory. The system consists of n processors (Pn) and m pieces of external memory (M1, M2, ..., Mm). Some processors share ...

Result # 8 Relevance:


Processor Communication Interface

1986-03-01

IPCOM000060245D

English

An interrupt-driven interface allows two central processing units (CPUs) having differing speeds to communicate with each other. The interface (Fig. 1) consists of an address bus 2, a control bus 3, interrupt lines 4, and a shared memory 5 that is ...

Result # 9 Relevance: 

Programmable Routing of Interrupts in a Multiprocessor Network

1982-08-01

IPCOM000051197D

English

A method to select under program control the routing of interrupts in a multiprocessor network of individual processors in a single processing system) is described below. Using one interrupt request can be routed to any set of the processors in a ...

Result # 10 Relevance: 

Transparent Virtual Memory

1983-01-01

IPCOM000045004D

English

A method is described whereby a computer may have an optional virtual memory capability installed or removed without modification of the operating system or of application code. The presence and operation of virtual memory is transparent to applications, as well ...

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Search Apparatus and methods are provided for transferring interrupts. One embodiment of a computing device includes a first processor, a memory in communication with the first processor, and computer executable instructions stored in memory and executable by the first processor. The computer executable instructions are provided to select an interrupt that has been waiting to be processed, for transfer from the first processor to one of other processors to select a second processor that has a short wait time for the interrupt, and transfer the interrupt from the first processor to the second processor.

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